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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/667,845	09/21/2000	Douglas A. Clark	F-208	1358

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PITNEY BOWES INC.
35 WATERVIEW DRIVE
P.O. BOX 3000
MSC 26-22
SHELTON, CT 06484-8000

EXAMINER

LANIER, BENJAMIN E

ART UNIT	PAPER NUMBER
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2132

DATE MAILED: 06/17/2004

4

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/667,845

Applicant(s)

CLARK, DOUGLAS A.

Examiner

Benjamin E Lanier

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 September 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 2.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 9, 10, 17, 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Piosenka, U.S. Patent 5,389,738. Referring to claims 1, 2, 9, 10, 17, 18, Piosenka discloses a tamperproof circuit device wherein an integrated circuit is shown (Fig. 4) to include three resistors in series with a wire loop between the first and second resistors and a wire loop between the second and third resistors, which meets the limitation of a trigger circuit including a plurality of resistors and a plurality of wire loops, the plurality of resistors including a first resistor, a second resistor and a third resistor, all of which being wired together in series and operatively connected to a power source, the plurality of wire loops including a first wire loop extending between the first resistor and the second resistor and a second wire loop extending between the second resistor and the third resistor, the first wire loop and the second wire loop being electrically isolated from each other but in physical proximity to each other so as to form a protective mesh that envelopes the protected integrated circuit. Piosenka also discloses detection circuitry to detect changes in voltage between the resistors due to possible breakage in the conducting path which indicates a possible attack on the circuit. Upon detection of the possible attack an alarm is triggered (Col. 3, lines 20-64 & Col. 4, lines 39-67), which meets the limitation of a detection circuit being in operative communication with the trigger circuit and the

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protected integrated circuit, the detection circuit monitoring a flow of current through the trigger circuit, wherein if the flow of current through the trigger circuit is altered because of an open condition in the first wire loop or the second wire loop or a short between the first wire loop and the second wire loop, then the detection circuit outputs a predetermined signal at a designated node, wherein if the first wire loop or the second wire loop are shorted to the ground layer, then the detection circuit outputs the predetermined signal.

Allowable Subject Matter

3. Claims 3-8, 11-16, 19-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art does not disclose connecting a transistor across the second resistor of a series of three in order to develop a bias voltage across the second resistor and having a second transistor connected across the first transistor and the ground in order to activate the second transistor by receiving output current from the first transistor.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin E Lanier whose telephone number is 703-305-7684. The examiner can normally be reached on M-Th 7:30am-5:00pm, F 7:30am-4pm.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron can be reached on (703)305-1830. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Benjamin E. Lanier



GILBERTO BARRÓN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100